I claim:

1. A system for providing parallel processing of data to a plurality of digital signal processors (DSPs), comprising:

means for transmitting communication data to a load management system from a CPU;

means for selecting a digital signal processor (DSP) from a plurality of DSPs for processing the communication data;

Sub A1

means for processing the communication data using the selected DSP; and

means for transmitting the processed data back to the CPU and to a communication device.

2. A system of claim 1, wherein the communication data is transmitted from a VoIP medium.

3. A system of claim 1, wherein the communication data is transmitted from a FoP medium.

4. A system of claim 1, wherein the communication data is transmitted from an IP to sonet medium.

5. A system of claim 1, wherein the communication data is transmitted from an encoder/decoder.

6. A system of claim 1, wherein the communication data is transmitted from a broadband communication medium.

7. A system of claim 1, wherein the communication data is transmitted from an image processing medium.

8. A system of claim 1, wherein the communication data is transmitted from

a data modem.

9. A system of claim 1, wherein the load management system comprises:

a plurality of direct memory access (DMA) devices having internal registers, a plurality of FIFOs, a plurality of state machines associated with the plurality of FIFOs, and a memory interface for interfacing the plurality of DMA devices with an external memory device;

a plurality of status and controls registers coupled to the plurality of DMA devices;

a CPU interface for interfacing the CPU with the plurality of status and control registers; and

a DSP interface for interfacing the plurality of DSPs with the plurality of DMA devices.

10. A system of claim 9, wherein the DSP interface includes a program/data memory and a ping-pong memory.

11. A system of claim 9 further comprising an external memory, wherein the external memory is coupled to the plurality of DSPs through dedicated memory threads.

12. A system of claim 9, wherein the CPU interface includes a routing MUX, wherein the routing MUX is coupled to the external memory device.

13. A system of claim 12, wherein the external memory device comprises a memory access controller array.

14. A system of claim 12, wherein the external memory device comprises a memory management system.

15. A DSP load management system, comprising:

a plurality of direct memory access (DMA) devices having internal registers, a plurality of FIFOs, a plurality of state machines associated with the plurality of FIFOs, and a memory interface for interfacing the plurality of DMA devices with an external memory device;

a plurality of status and controls registers coupled to the plurality of DMA devices;

a CPU interface for interfacing a CPU with the plurality of status and control registers; and

a DSP interface for interfacing a plurality of DSPs with the plurality of DMA devices.

16. A DSP load management system of claim 15, wherein the external memory device comprises a memory access controller array.

17. A DSP load management system of claim 15, wherein the external memory device comprises a memory management system.

18. A DSP load management system of claim 15 further including a decoder for decoding instructions from the CPU.

19. A DSP load management system of claim 18, wherein the instructions include load and algorithm switching instructions in the plurality of DSPs.

20. A DSP load management system of claim 19, wherein the load and algorithm switching instructions provides optimal processing of the plurality of DSPs.

21. A method of providing parallel processing of data to a plurality of digital signal processors (DSP), the method comprising:

transmitting communication data to a central processing unit (CPU);

writing the communication data to a selected register from a plurality of registers in a load management system, wherein each register is coupled to a DSP via a designated thread;

transmitting the communication data from the selected register to its corresponding DSP via the designated thread; and

processing the communication data using the corresponding DSP.

22. A method of claim 21, wherein the register is selected based on the current load status of the plurality of registers.

23. A method of claim 22, wherein the register is selected based on the algorithms loaded in the plurality of registers.

24. A method of claim 21, wherein the communication data is loaded into the register having the least load and same algorithm as the new load.

25. A method of claim 21, wherein the communication data is loaded into the register after switching the load from the register into a second register.

26. A method of claim 21, wherein the plurality of registers includes at least two different algorithms.

27. A method of claim 21, wherein the plurality of registers includes at least three different algorithms.

28. A method of claim 21 further comprising simultaneously processing data using the plurality of DSPs.

29. A method of claim 21, wherein the communication data is transmitted from one of a VoIP medium, a FoP medium, an IP to sonet medium, an encoder/decoder, a broadband communication medium, an image processing medium, and a data modem.

30. A method of selecting a particular DSP from a plurality of DSPs for loading a new load, the method comprising:

analyzing the current loads and algorithms associated with each DSP; and

selecting the particular DSP from the plurality of DSPs based on the current loads and algorithms, wherein the selected DSP has a least load and includes the same algorithm as the new load.

31. A method of optimizing the processing capabilities of a plurality of digital signal processors (DSPs) on an SOC device having a DSP load management system (DLMS), comprising:

transmitting communication data to a central processing unit (CPU);

writing the communication data to a selected register from a plurality of registers in a load management system, wherein each register is coupled to a DSP via a designated thread;

transmitting the communication data from the selected register to its corresponding DSP via the designated thread, wherein the corresponding DSP is the least loaded DSP on frame bourndaries; and

processing the communication data using the corresponding DSP.

32. A method according to claim 31, wherein the DLMS provides inter-transaction optimization, intra-transaction optimization, and hardware mapping optimization.